REMARKS

The Office Action mailed July 31, 2008, and the references cited by the Examiner have been carefully reviewed by Applicant.

Claims 1-28 are pending.

Claims 13-28 have been withdrawn.

Claims 6 -12 are allowed.

Claims 1-4 are rejected.

Claim 5 is objected to, but would be allowable if rewritten in independent form.

Applicant has made certain amendments to claim 1. Applicant respectfully submits that, based on these amendments and for the reasons stated herein, this application is in condition for allowance.

Rejection of Claims

In the Office Action mailed July 31, 2008, the Examiner rejected Claims 1-4 under 35 USC § 102(b) as being anticipated by U.S. Patent No. 5,572,695 (*Andrews*).

Regarding claim 1, Applicant submits that *Andrews* fails to disclose or suggest physical channels corresponding to cabling wires. Amended claims 1 reads (bold added for ease of identification):

1. An adapter channel mapping system for mapping channels of a network, comprising:

a memory component operable to communicate with the network and having a first memory portion and a second memory portion, the first memory portion operable to communicate with **a first physical channel of the network corresponding to at least a first cabling wire** and the second memory portion operable to communicate with **a second physical channel of the network corresponding to at least a second cabling wire**; and

a mapping component operable **to map each one of the first and second memory portions to one of the first and second physical channels** based on a first configuration of the network and further operable **to map each one of the first and second memory portions to one of the first and second physical channels** based on a second configuration of the network.

As shown above, claim 1 recites that the memory portions communicate with **physical channels of the network corresponding to cabling wires**. Specifically, the present application discloses a system for testing a network (LAN) cabling wires. The system comprises physical channels connected to the cabling wires. *See* application, [0030]. The physical channels are memory locations or input/output registers used to transmit, receive, and/or store signals or data associated with the network, via the cabling wires. Additionally, the system comprises memory portions or memory locations, which provide logical channels for storing addresses or references to the physical channels. *See* application, [0034]. The memory portions communicate with the physical channels, for instance via a read/write module. *See* application, [0035]. Accordingly, the memory portions communicate with the physical channels to effectively cross pairs of cabling wires, based on a configuration, by remapping the addresses of the physical channels corresponding to the cabling wires. *See* application [0033].

In contrast, *Andrews* discloses memory portions in communication with **channels that do not correspond to cabling wires**. Specifically, *Andrews'* discloses a system for accessing more memory addresses than is logically allowable using a memory mapping mechanism. *See Andrews*, Col 2, ll. 40-43. The system comprises DSP memory portions (53, 56, 58 and 60 in Fig. 4) that are mapped to some DRAM memory regions (64, 68, 70, 72, 74, and 76 in Fig. 4), including channel areas or regions, based on the memory mapping mechanism. *See Andrews*, Col 8, ll. 5-30. As such, the memory mapping mechanism allows the DSPs to access and connect to more DRAM memory locations than the maximum allowed by the DSPs addressing bits. *See Andrews*, Col 7, ll. 26-31. However, *Andrews* does not disclose, teach, or suggest that the DSPs and the DRAM connect, use, or any way relate to cabling wires. Since *Andrews* does not disclose that the channels are connected to cabling wires or are associated with cabling wires, Applicant submits that claim 1 is allowable.

Further, claim 1 recites that **each one memory portion is mapped to one physical channel** based on a network configuration. Specifically, the applicant discloses a one-to-one memory mapping scheme that maps each one of two memory portions to one of two physical channels based on one of two configurations or possibilities. In contrast, *Andrews* discloses **a plurality of memory portions are mapped to at least one channel**. *Andrews'* mapping mechanism maps a DSP memory portion (53, 56, 58 or 60 in Fig. 4) of each DSP, and hence a plurality of DSP memory portions, to a at least one DRAM memory region (64, 68, 70, 72, 74, or 76 in Fig. 4) based on one of three modes. In a first mode (Mode 1), the DSP memory portion 52 of each DSP is mapped to the DRAM memory region 64, the DSP memory portion 58 of each DSP is mapped to the four DRAM memory regions 68, and the DSP memory portion 60 of each DSP is mapped to the four DRAM memory regions 70. *See Andrews*, Col 8, ll. 46-51. Similarly,

in a second mode (Mode 2) and third mode (Mode 3), the mapping mechanism maps a plurality of DSP memory portions to at least one DRAM physical memory region. *See Andrews*, Col 8, ll. 55-62, Col 9, ll. 28-36. Therefore, *Andrews* discloses a multiple-to-multiple or multiple-to-one memory mapping scheme that maps a plurality of DSP memory portions, and not each one DSP memory portion, to at least one DRAM physical memory region, and not to one DRAM physical memory region. Thus Andrews does not disclose the present invention as claimed in claim 1 for mapping each one of the memory portions to one of the physical channels. For this additional reason, Applicant submits that claim 1 is allowable.

Since all the elements of the claim 1 are not disclosed by *Andrews*, as discussed above, Applicant submits that claim 1 and dependent claims 2-4 be allowed.

Allowable Claims

The Examiner indicated that claim 5 was objected to, but would be allowed if rewritten in independent form. Applicant submits that claim 5, which depends from allowable claim 1, is now in condition for allowance.

The Examiner allowed claims 6-12. Applicant appreciates the Examiner's allowance of these claims.

CONCLUSION

Applicant respectfully submits that the application, in its present form, is in condition for allowance. If the Examiner has any questions or comments or otherwise feels it would be helpful in expediting the application, the Examiner is encouraged to telephone the undersigned at (972) 731-2288. Applicant intends this communication to be a complete response to the Office Action mailed July 31, 2008.

The Commissioner is hereby authorized to charge payment of any fee associated with any of the foregoing papers submitted herewith to Deposit Account No. 50-1515, Conley Rose, P.C.

Respectfully submitted,
CONLEY ROSE, P.C.

Date: October 31, 2008

J. Robert Brown, Jr.
Reg. No. 45,438

ATTORNEY FOR APPLICANTS

5601 Granite Parkway, Suite 750
Plano, Texas 75024
Telephone: (972) 731-2288
Facsimile: (972)731-2289